DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/22/2008 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities: in line 12, the term "greatest" is vague. The examiner assumes that applicant has intended to mean "more". Appropriate correction is required.

3. Claim 1 is objected to because of the following informalities: In lines 13-14, a phrase "free of contact with the first chip and the semiconductor package" is vague, because figure 6b shows that the hollow parts are on top of the package 33. The examiner assumes in this Office Action that applicant has intended to mean free of contact with the first chip. Appropriate correction is required.

4. Claim 8 is objected to because of the following informalities: the limitation in claim 8 fails to provide further structurally limit of the device. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4, and 6-8, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ku (US 2004/0099945)

Ku discloses a multi-chip package device with a heat sink 50 (fig. 4), comprising a chip carrier 10 (fig.4); at least one first chip 30 (fig. 4) or 31 (fig. 4) mounted on and electrically connected to a surface of the chip carrier 10; at least one semiconductor package 20 (fig. 4) mounted on and electrically connected to the surface of the chip carrier 10 (fig. 4); and the heat sink 50 (fig. 4) mounted via an adhesion layer (page 4, [0061], lines 3-5) on a surface of the first

chip 30, 31 (fig. 4) and a surface of the semiconductor package 20 (fig. 4) that are opposite to surfaces of the first chip 30, 31 (fig. 4) and the semiconductor package 20 mounted on the chip carrier 10 (fig. 4), wherein a plurality of hollow parts 504 (fig. 4) extending through the heat sink 50 are formed at a location of the heat sink subjected to more thermal stresses, and the plurality of the heat sink are formed symmetrically at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stresses from the heat sink . It is noted that the hollow parts 504 (fig. 4) of the heat sink are not positioned on the chips and the package to release heat from the device and that the heat sink 50 adheres tot eh chip with glue connection (paragraph [0061]) .

Further, it is noted that the term "formed" or "formed symmetrically" in lines 11-13 of the claim 1 provokes a product-by-process recitation. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 777 F. 2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding to the recitation where the location of the hollow parts being subjected to more thermal stresses, it is interpreted as a functional language because the recitation does not result in further limiting the structure of the device. Note that it has been held that a recitation with respect to the manner in which a claimed device is intended to be employed does not differentiate the claimed device from a prior art device satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F. 2d 1647 (1987).

As to claim 2, Ku teaches that the semiconductor package 20 (fig. 4) is a flip-chip ball grid array package (specification, page 1, [0004]).

As to claim 3, Ku teaches that the first chip 30 or 31 (fig. 4) is capable of being a graphic chip.

As to claim 4, Ku teaches that the first chip 30 or 31 (fig. 4) is capable of being a graphic processing unit.

As to claim 6, Ku teaches that the first chip 30 or 31 (fig. 4) is mounted at the center of the chip carrier 10 (fig. 4), and the semiconductor package 20 is mounted at a position on the chip carrier 10 corresponding to a corner of the heat sink 50.

As to claim 7, Ku teaches that at least one pair of the semiconductor packages 20 (fig.4) are mounted on the chip carrier 10 (fig. 4), and the hollow part 504 (fig. 4) of the heat sink 50 (fig. 4) is located between the semiconductor packages.

As to claim 8, at least one symmetrical pair (fig. 4) of the hollow parts 504 (fig. 4) are formed through the heat sink 24(fig.4).

As to claim 19, Ku discloses the invention substantially as claimed, except the size of the hollow parts being adjusted depending on a thickness of the heat sink. However, Ku discloses a general size and thickness of the heat sink. Accordingly, it would have been obvious to one of ordinary skill in art to use the heat sink teaching of Ku in a way as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233,235 (CCPA 1955). Also, it is noted that when the heat sink's

thickness increases, the size of the hollow parts are also increased as well because the depth of the hollow parts are deeper.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ku in view of Chee et al. (2003/0089977; hereinafter as Chee).

Ku discloses the invention substantially as claimed. However, Ku does not explicitly teach that the semiconductor package is a Random Access Memory (RAM) unit.

Chee discloses an analogous multi-chips BGA package (fig. 3b) having a carrier 314, and chips 311, 312, 313 (fig. 3b), wherein the package includes a RAM unit (paragraph [0023]).

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to construct the package for multi-chips of Ku to include a RAM unit, as taught by Chee, for reducing packaging cost (paragraph [0013]).

6. Claims 1-8, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) (figure 2) in view of Ku (US 2004/0099945).

APA discloses a packaging device having a carrier 20, a first chip 21, a package 22 electrically connected to the first chip 21 (see figure 2), and a heat sink 24 mounted via an adhesion layer 23 on the surface of the first chip and the package.

However, APA does not explicitly teach a plurality of hollow parts extending through the heat sink.

Ku discloses a multi-chip package device with a heat sink 50 (fig. 4), comprising a chip carrier 10 (fig.4); at least one first chip 30 (fig. 4) or 31 (fig. 4) mounted on and electrically connected to a surface of the chip carrier 10; at least one semiconductor package 20 (fig. 4) mounted on and electrically connected to the surface of the chip carrier 10 (fig. 4); and the heat

sink 50 (fig. 4) mounted via an adhesion layer (page 4, [0061], lines 3-5) on a surface of the first chip 30, 31 (fig. 4) and a surface of the semiconductor package 20 (fig. 4) that are opposite to surfaces of the first chip 30, 31 (fig. 4) and the semiconductor package 20 mounted on the chip carrier 10 (fig. 4), wherein a plurality of hollow parts 504 (fig. 4) extending through the heat sink 50 are formed at a location of the heat sink subjected to more thermal stresses, and the plurality of the heat sink are formed symmetrically at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stresses from the heat sink . It is noted that the hollow parts 504 (fig. 4) of the heat sink are not positioned on the chips and the package to release heat from the device and that the heat sink 50 adheres tot eh chip with glue connection (paragraph [0061]) .

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the heat sink of APA with the hollow parts, as taught by Ku, for reducing the cost and improving the heat dissipation (paragraph [0013]).

Further, it is noted that the term "formed" or "formed symmetrically" in lines 11-13 of the claim 1 provokes a product-by-process recitation. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 777 F. 2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding to the recitation where the location of the hollow parts being subjected to more thermal stresses, it is interpreted as a functional language because the recitation does not result in further limiting the structure of the device. Note that it has been held that a recitation with

respect to the manner in which a claimed device is intended to be employed does not differentiate the claimed device from a prior art device satisfying the claimed structural limitations. *Ex Parte Masham,* 2 USPQ F. 2d 1647 (1987).

As to claim 2, APA teaches that the semiconductor package 22 (fig. 2) is a flip-chip ball grid array package.

As to claim 3, APA teaches that the first chip 21 (fig. 2) is capable of being a graphic chip.

As to claim 4, APA teaches that the first chip 21 (fig.2) is capable of being a graphic processing unit.

As to claim 5, APA teaches that the chip 21 is a RAM.

As to claim 6, APA teaches that the first chip 21 (fig. 2) is mounted at the center of the chip carrier 20 (fig. 2), and the semiconductor package 20 is mounted at a position on the chip carrier 10 corresponding to a corner of the heat sink 24.

As to claim 7, similar to the rejection of claim 1above, APA teaches that at least one pair of the semiconductor packages 22 (fig.2) are mounted on the chip carrier 20, and Ku's hollow part 504 (fig. 4) of the heat sink 50 (fig. 4) is located between the semiconductor packages.

As to claim 8, similar to the rejection of claim 1 above, Ku discloses at least one symmetrical pair (fig. 4) of the hollow parts 504 (fig. 4) are formed through the heat sink 24(fig.4).

As to claim 19, APA and Ku disclose the invention substantially as claimed, except the size of the hollow parts being adjusted depending on a thickness of the heat sink. However, APA and Ku disclose a general size and thickness of the heat sink. Accordingly, it would have

been obvious to one of ordinary skill in art to use the heat sink teaching of APA and Ku in a way as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233,235 (CCPA 1955). Also, it is noted that when the heat sink's thickness increases, the size of the hollow parts are also increased as well because the depth of the hollow parts are deeper.

Response to Arguments

7. Applicant's arguments filed 08/25/2008 have been fully considered but they are not persuasive.

In the remarks, applicants argue that Ku fails to overcome the newly amended portions of claim 1. As stated in the rejection above, Ku anticipates all of the limitation in claim 1. Thus, claim 1 is still rejected. (See above rejection).

In general, a heat sink in the semiconductor device is to release heat from the device. The apertures in the heat sink allow the production of the device to reduce the cost. This is an advantage in the manufacturing production of the semiconductor device. Thus, applicant's argument that the apertures of Ku are not capable of releasing thermal stresses, the examiner respectfully disagrees. The apertures of Ku are capable of releasing thermal stresses by providing an escape route for the heat built-up in the device.

For the foregoing reasons, applicant still has not overcome the cited references.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to (Vikki) Hoa B. Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Ms. Davienne Monbleau, can be reached at (571) 272-1945. The office fax number is 571-273-8300.

Any request for information regarding to the **status** of an application may be obtained from the **Patent Application Information Retrieval (PAIR) system**. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications have ceased to be mailed to applicants with Office actions since June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at **http://www.uspto.gov/ebc/index.html** or 1-866-217-9197 for information on this policy.

Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

/(Vikki) Hoa B Trinh/

Examiner, Art Unit 2893